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FINAL TECHNICAL REPORT

GaAs WAVEGUIDE DETECTOR ARRAY

FOR AN IOC SPECTRUM ANALYZER

December 21, 1978

by

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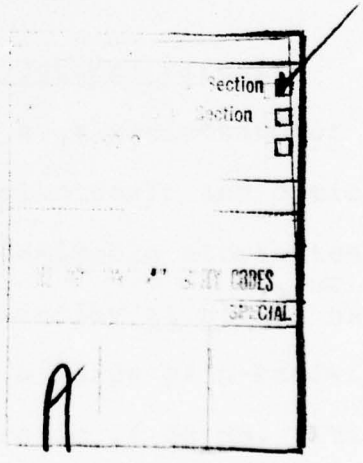

GaAs WAVEGUIDE DETECTOR ARRAY FOR AN IOC SPECTRUM ANALYZER

1. INTRODUCTION

Integrated optical circuits (IOC's) combining optical signal propagation with high-speed photoelectronic detection have a high potential for very fast analog or digital signal processing. A wideband, real-time spectrum analyzer using thermally grown oxides on a silicon substrate has been investigated by Anderson[1]. Sun et al.[2] have demonstrated the feasibility of a 3-channel time demultiplexing scheme. Data rates of 1 Mbps have been achieved using GaAs waveguide detectors, and frequency demultiplexing has also been investigated.

1.1 Suitability of GaAs for Integrated Optical Circuits

Gallium Arsenide shows great promise as a semiconductor for use in IOC fabrication. A large variety of electronic and optical devices have been demonstrated in GaAs with the desirable attributes of high speed, low noise, and high efficiency. Lindley et al.[3] have fabricated avalanche photodetectors with a large gain-bandwidth product (<50 GHz) and a signal-to-noise ratio of 30 dB. Stillman et al.[4] have fabricated GaAs waveguides which operate with attenuation as low as 2 cm^{-1} at GaAs laser wavelengths. In addition, GaAs-AlGaAs double heterostructre lasers emitting at 9100 Å have

been integrated with high-purity GaAs waveguides[5]. Electro-absorption avalanche photodiode (EAP) detectors make use of the Franz-Keldysh effect to detect optical signals at frequencies beyond the normal absorption edge of GaAs [2,6-8]. Their use as an output stage provides the key to monolithic integration of optical circuits in GaAs: that is, with EAP devices signal generation, propagation, processing, and optoelectronic decoding are possible on a single substrate.

1.2 Application to Spectrum Analysis

One application for such a monolithic IOC is real-time, wide-bandwidth spectrum analysis. A hypothetical configuration for an integrated GaAs spectrum analyzer is shown in Figure 1. A distributed feedback[9], distributed Bragg reflector[10], or integrated Fabry-Perot[5] laser is used as a coherent optical source. Acousto-optical[11,12] or electro-optical[13] deflection is used to encode the RF signal to be processed. The encoded signal is Fourier transformed by a Fresnel[14] or Luneburg[1] lens. The resulting spectrum is collected by an array of integrated channel waveguides terminated in EAP detectors, and these detectors decode the optical information, converting it into compatible electrical information. The signal level is regulated by on-chip automatic gain control (AGC) to increase the dynamic range. The final signal is fed to an array of charge coupled devices[15] for multiplexed output.

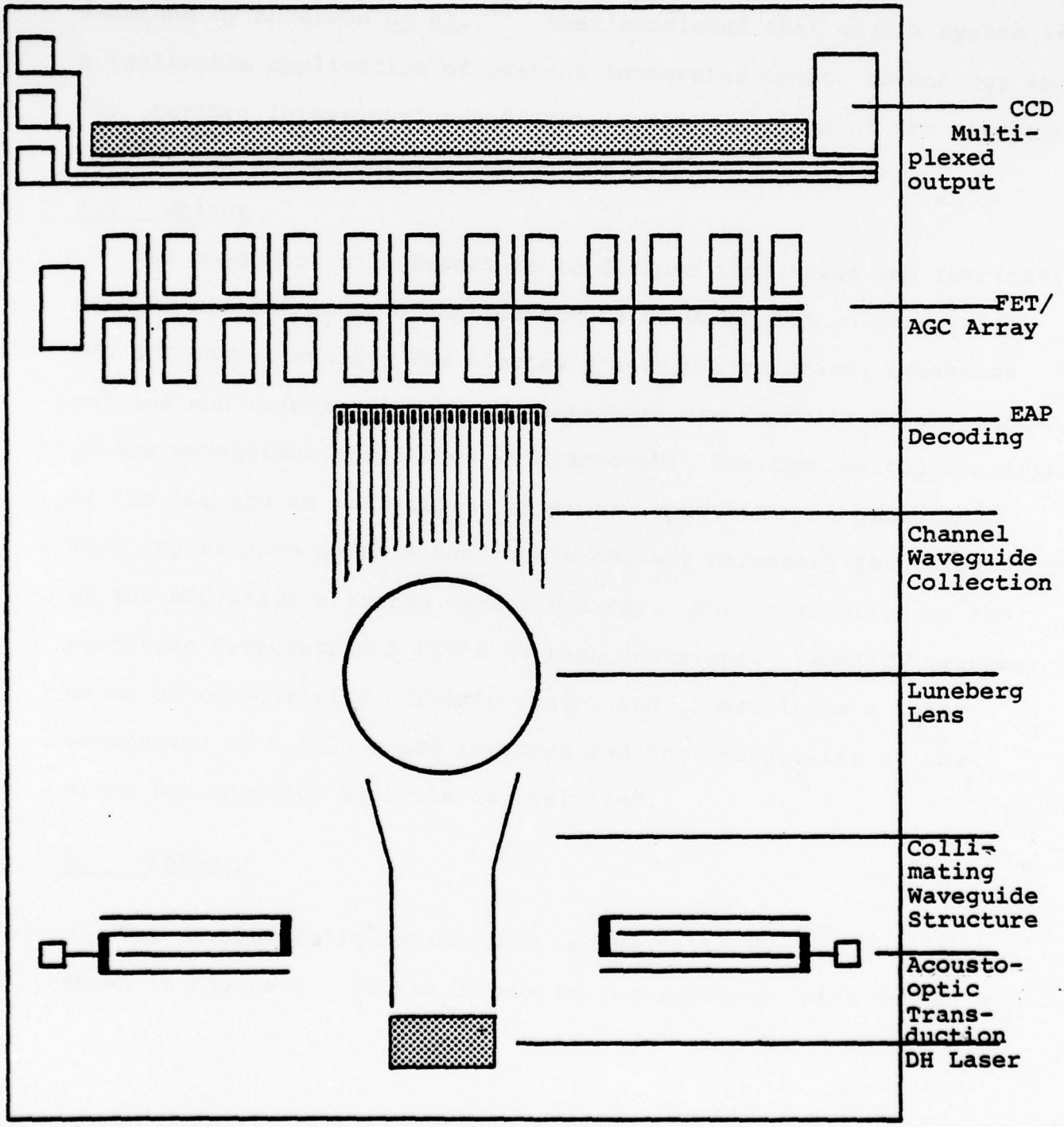

Fig. 1. A Hypothetical GaAs Ioc for real-time Spectrum Analysis.

The requirements for such an IOC spectrum analyzer have been examined by Anderson et al..[1] They concluded that such a system is a realizable application of present integrated optics technology in Si. Further investigation and experimental development are necessary, however, to assure optimum design and performance.

1.3 Object

The object of this report is to discuss the design and fabrication of a 20-element array of EAP detectors in GaAs with an integrated FET AGC output stage. The electric field distribution, breakdown voltage and responsivity of the detectors are calculated, and guiding in the waveguides structures is discussed. The theoretical operation of the AGC and an analytic model of its operation are presented. This report also details the double epitaxy necessary for integration of the AGC stage with the detector array. The fabrication of the waveguide detectors and FET's is then described. Finally, measurements of responsivity, dynamic range, and crosstalk at a laser wavelength of 0.905 μm are reported and the suitability of the array for spectrum analysis is evaluated.

2. ANALYSIS

The device configuration used in the following analyses is shown in Figure 2. At the bottom is the substrate with doping N_s.

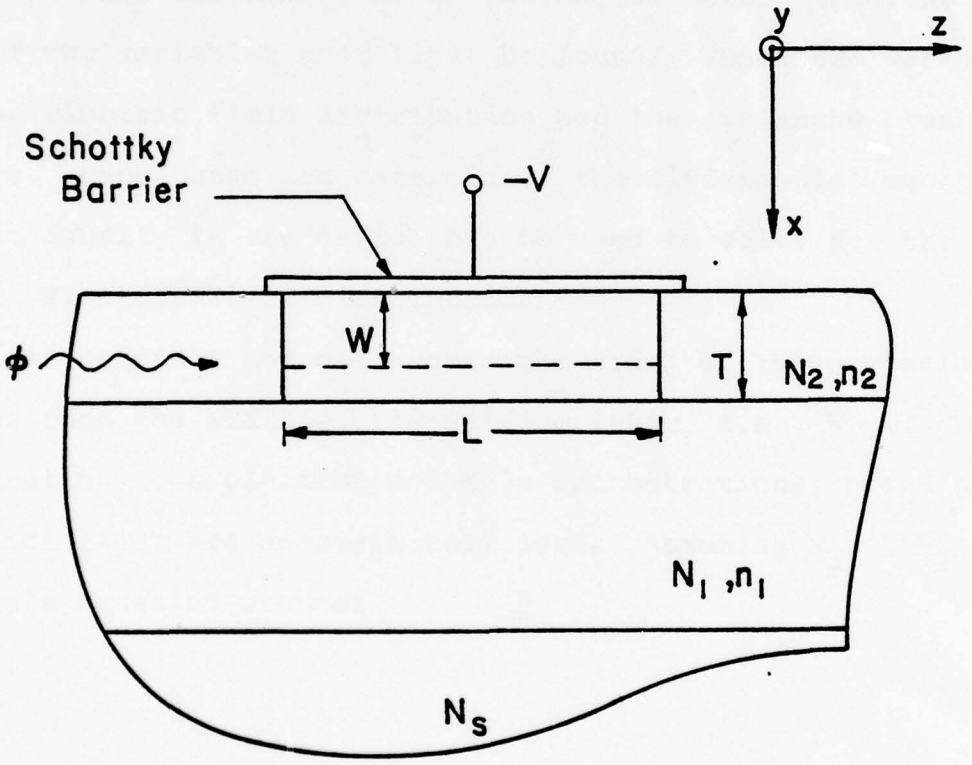

Fig 2. Schematic Device Configuration for Analysis of EAP Detectors.

On top of this substrate are two epitaxial layers doped at N_1 and N_2, with refractive indices n_1 and n_2. The thickness of the top (waveguide) layer is denoted by T and the depletion width for an applied voltage, -V, is W. The length of the device is L.

2.1 The EAP Detector

To examine the operation of the EAP detector, the functional form of two variables must first be found. These two variables are the electric field distribution and the avalanche breakdown voltage. Once these are determined, the differential equations for current density in the device can be used to solve for the responsivity.

2.1.1 Electric Field Distribution

First consider the case where the width of the depletion region is less than the width of the guiding layer, i.e., $W < T$. With no illumination, the electron and hole concentrations, n and p, in the depletion layer are approximately zero. Assuming $N_d^+ \cong N_2$, Poisson's Equation becomes

$$\frac{dE}{dx} = \frac{q}{\varepsilon} N_2 \quad , \tag{2.1.1}$$

and

$$E = \frac{q}{\varepsilon} N_2 x + C_1 \quad . \tag{2.1.2}$$

By defining the depletion layer width as the point where the electric field vanishes, we have $E = 0$ at $x = W$. Then,

$$E = \frac{q}{\varepsilon} N_2 (x - W) \tag{2.1.3}$$

We can now find W in terms of V, the applied voltage. Integrating

$$E = -\frac{d\psi}{dx} = \frac{q}{\varepsilon} N_2 (x - W) \qquad (2.1.4)$$

gives the potential, ψ, as

$$\psi(x) = \frac{qN_2}{\varepsilon} \left(xW - \frac{x^2}{2}\right) + C_2 \quad . \qquad (2.1.5)$$

Defining $\psi(0) \equiv -V$,

$$\psi(x) = \frac{q}{\varepsilon} N_2 \left(Wx - \frac{x^2}{2}\right) - V \quad . \qquad (2.1.6)$$

We know that $\psi(W) = 0$. Therefore,

$$V = \frac{q}{\varepsilon} N_2 \frac{W^2}{2} \quad , \qquad (2.1.7)$$

or,

$$W = \left(\frac{2\varepsilon}{qN_2} V\right)^{1/2} \quad , \qquad (2.1.8)$$

We finally obtain the closed form

$$E(x) = \frac{q}{\varepsilon} N_2 x - \frac{2V}{W} \quad . \qquad (2.1.9)$$

The case that remains to be discussed is when the width of the depletion region equals or exceeds the width of the guiding layer. If N_1 is a conducting layer and $N_2 \ll N_1$ to provide waveguiding (see Section 2.2.2), then $W \cong T$ and $E(W) \neq 0$. We have the solution from (2.1.2):

$$E(x) = \frac{qN_2}{\varepsilon} x + E(o) \tag{2.1.10}$$

From (2.1.4),

$$\psi(W) = -TE(o) - \frac{qN_2}{2\varepsilon} T^2 = V \tag{2.1.11}$$

Defining the pinch-off voltage V_p such that $E(T) = 0$,

$$V_p = \frac{qN_2T^2}{2\varepsilon} \tag{2.1.12}$$

Therefore,

$$E(o) = - \frac{(V + V_p)}{T} \tag{2.1.13a}$$

$$E(w) = - \frac{(V - V_p)}{T} \quad , \tag{2.1.13b}$$

and our solution is

$$E(x) = \frac{q}{\varepsilon} N_2 x - \frac{(V + V_p)}{T} \quad . \tag{2.1.14}$$

Equations (2.1.9) and (2.1.14) are those required to calculate the breakdown voltage and responsivity.

2.1.2 Avalanche Breakdown

The avalanche breakdown analysis presented by Sun et al.,[2] applies directly to the waveguide detectors reported here. The condition for breakdown is determined by the continuity equations for electron and hole currents:

$$\frac{dJ_n(x)}{dx} = \alpha_n J_n(x) + \alpha_p J_p(x) \qquad (2.1.15a)$$

$$\frac{dJ_p(x)}{dx} = -\frac{dJ_n(x)}{dx} \quad . \qquad (2.1.15b)$$

The α_n and α_p are the ionization coefficients for electrons and holes respectively. In GaAs these ionization coefficients are unequal and highly field dependent[16]. This leads to the field-dependent breakdown conditions,

$$\int_o^T \alpha_p \exp\left[\int_x^T (\alpha_n - \alpha_p)dx'\right]dx = 1 \quad , \qquad (2.1.16a)$$

and

$$\int_o^T \alpha_n \exp\left[-\int_o^x (\alpha_n - \alpha_p)dx'\right]dx = 1 \quad , \qquad (2.1.16b)$$

which are equivalent.

The breakdown voltages for GaAs EAP detectors have been calculated as a function of layer thickness for various doping levels. The results of these calculations are shown in Figure 3. These plots were generated using the electric fields given by Equations (2.1.9) and (2.1.14). The ionization coefficients used in calculating these

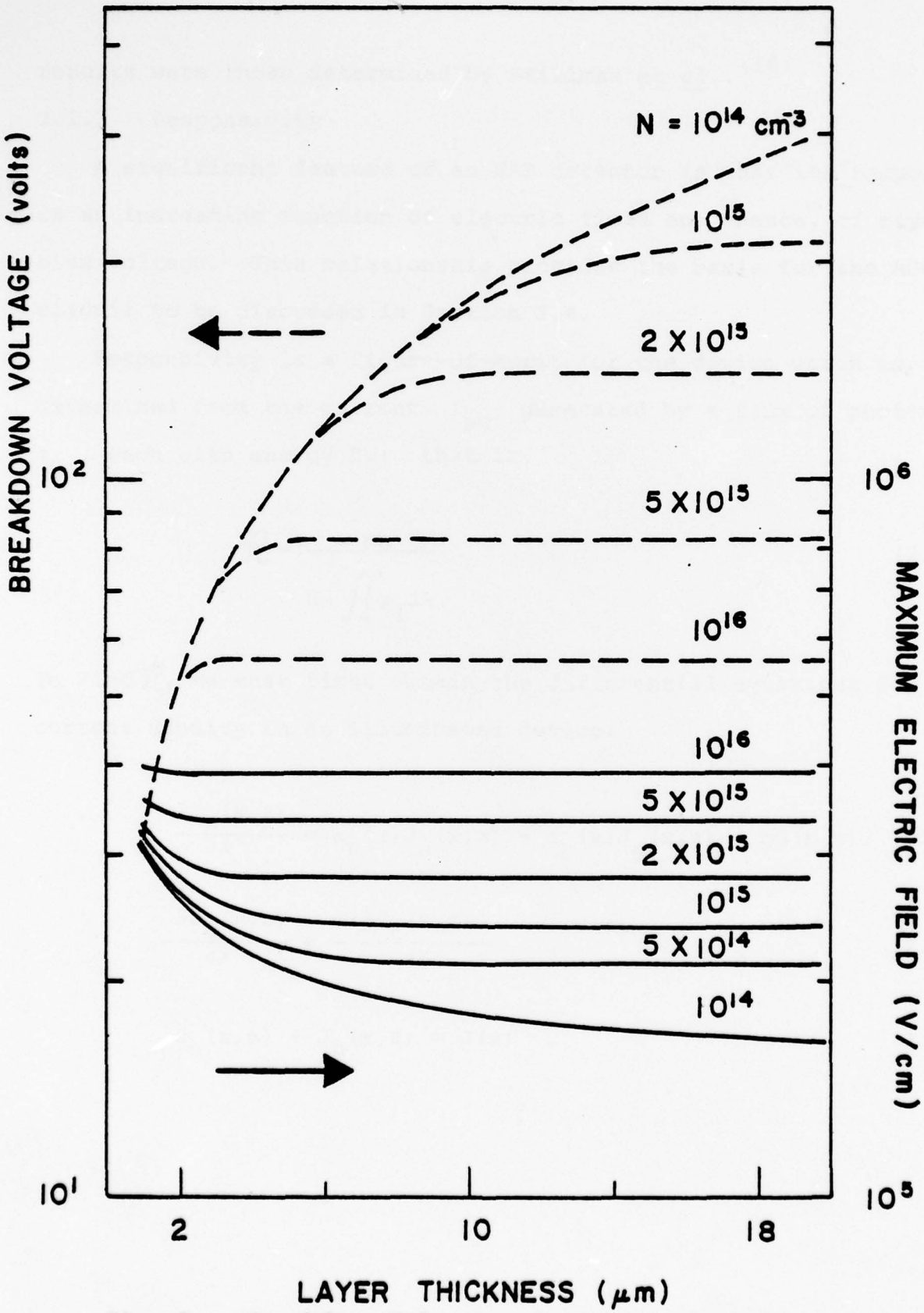

Fig. 3. Breakdown Voltage and Maximum Electric Field of GaAs EAP Waveguide Detectors as a Function of Layer Thickness and Doping Level.

results were those determined by Stillman et al..[16]

2.1.3 Responsivity

A significant feature of an EAP detector is that its responsivity is an increasing function of electric field and, hence, of reverse bias voltage. This relationship provides the basis for the AGC circuit to be discussed in Section 2.4.

Responsivity is a figure-of-merit for the device which is determined from the current, I_{ph}, generated by a flux of photons, ϕ_q, each with energy $\bar{h}\omega$: that is,

$$\mathcal{R} = \frac{I_{ph}}{\bar{h}\omega \iint \phi_q dA} \quad . \tag{2.1.17}$$

To Find $\mathcal{R}$, we must first obtain the differential equations for the current density in an illuminated device:

$$\frac{\partial J_n(x,z)}{\partial x} = \alpha_n(x) J_n(x,z) + \alpha_p(x) J_p(x,z) + qG(x,z), \tag{2.1.18a}$$

$$\frac{\partial J_p(x,z)}{\partial x} = - \frac{\partial J_n(x,z)}{\partial x} \quad , \tag{2.1.18b}$$

$$J_n(x,z) + J_p(x,z) = J(z) \quad . \tag{2.1.18c}$$

The α_n and α_p are now x-dependent due to gradients in the electric field caused by the illumination. The function G(x,z) is defined to be the generation rate of optically-excited electron-hole pairs. From this it is evident that

$$G(x,z) = -\frac{\partial \phi(x,z)}{\partial x} \quad . \tag{2.1.19}$$

The photon flux density, $\phi(x,z)$, is given by

$$\phi(x,z) = \phi_i(x)e^{-\Gamma z} \tag{2.1.20}$$

where Γ is the equivalent electroabsorption coefficient. Considering (2.1.19) and (2.1.20) together, we can write

$$G(x,z) = \alpha(x)\phi_i(x)e^{-\Gamma z} \tag{2.1.21}$$

where $\alpha(x)$ is defined to be the Franz-Keldysh electroabsorption coefficient. From (2.1.18), using the integrating factor,

$$P(\Lambda) = \exp\left[-\int_o^{\Lambda} \{\alpha_n(\Lambda') - \alpha_p(\Lambda')\}d\Lambda'\right] \quad , \tag{2.1.22}$$

we obtain

$$J_n(x,z) = \frac{\int_o^x \left[J(z)\alpha_p(x') + qG(x',z)\right]P(x')dx' + J_n(o,z)}{P(x)} \tag{2.1.23}$$

Since J(z) is independent of x' , it can be taken out of the first integral. From (2.1.18c),

$$J_n(W,z) = J(z) - J_p(W,z) \quad . \tag{2.1.24}$$

Therefore,

$$J(z) = \frac{q\int_o^W G(x,z)P(x)dx + J_p(W,z)P(W) + J_n(o,z)}{P(W) - \int_o^W \alpha_p(x)P(x)dx} \quad . \tag{2.1.25}$$

The responsivity can now be written as

$$R = \frac{\int_o^L J(z)dz}{q\int_{-oo}^{oo} \bar{h}\omega\phi_i(x)dx} \quad , \tag{2.1.26}$$

for a device of length L.

Sun et al.,[2] have calculated equivalent electroabsorption coefficients, Γ, for EAP waveguide detectors. Plots of responsivity using their results are shown in Figure 4. Values are normalized to the breakdown voltage, V_B.

2.2 Waveguides

A cross-section of the waveguide structure of interest is shown in Figure 5. The waveguides are of the etched-channel variety,

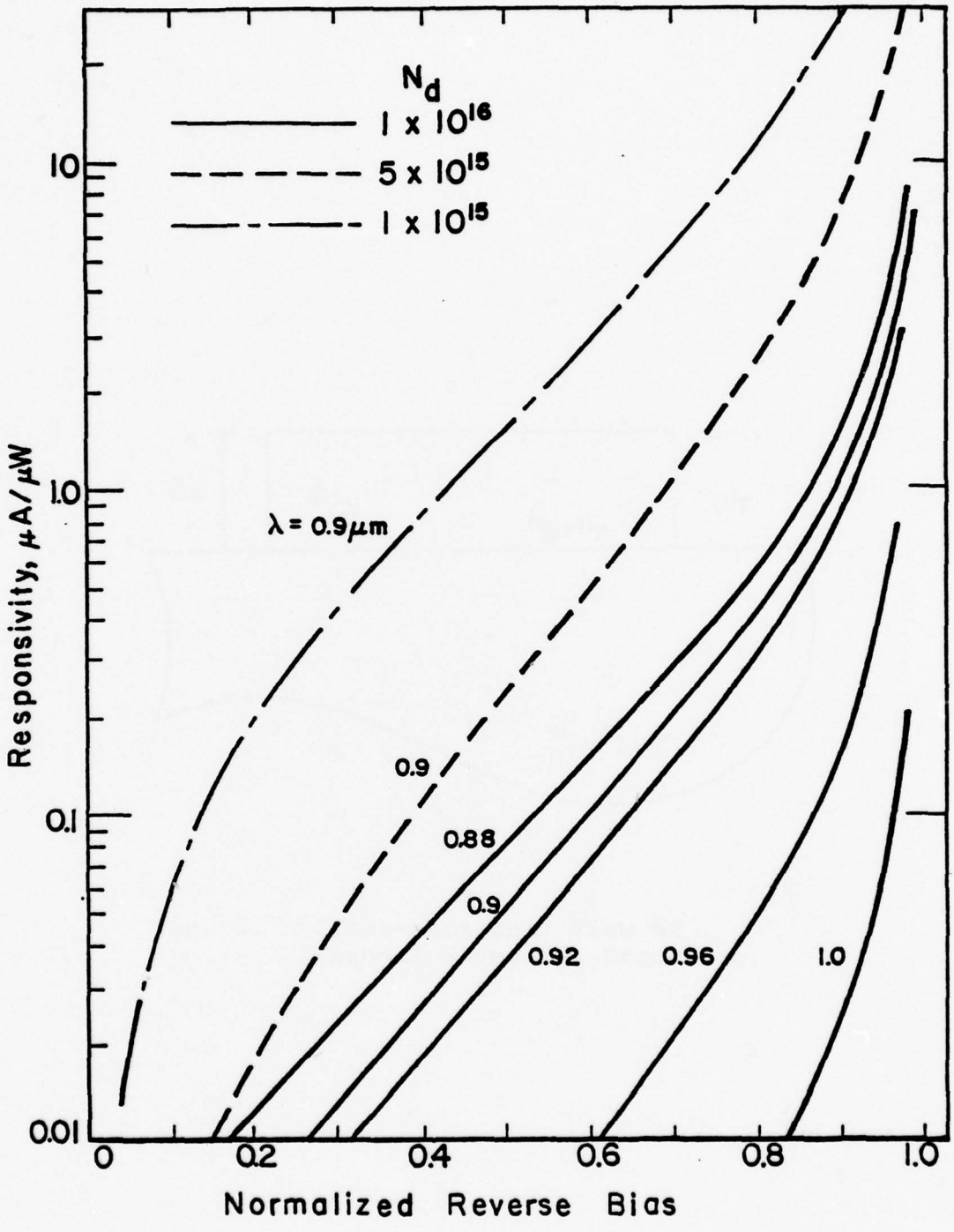

Fig. 4. Calculated Responsivity as a Function of Bias, Wavelength, and Doping Level for a 100 μm Long EAP Detector.

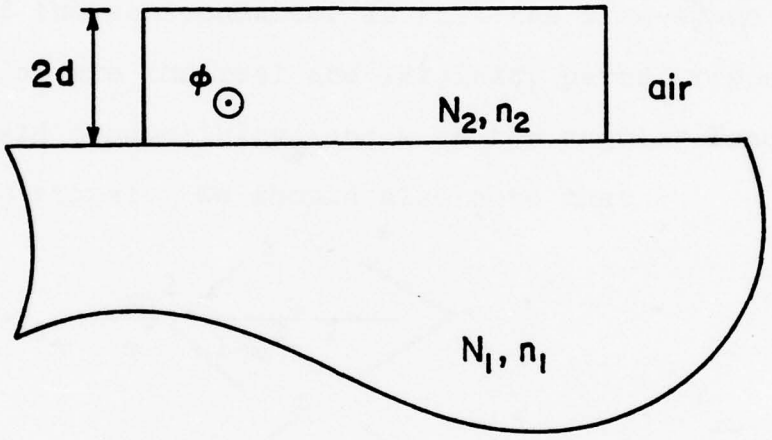

Fig. 5. Cross-sectional View of Channel Waveguide Structure.

and the layers are doped such that $N_2 << N_1$.

2.2.1 Difference in Index of Refraction

The index of refraction, n, of a semiconductor is given approximately by the expression

$$n^2 \cong \frac{1}{2}(\varepsilon_R - \frac{\sigma_i}{\omega\varepsilon_o}) + \frac{1}{2}[(\varepsilon_R - \frac{\sigma_i}{\omega\varepsilon_o})^2 + \frac{\sigma_r^2}{\omega^2\varepsilon_o^2}]^{1/2} \qquad (2.2.1)$$

obtained from the Kramers-Kronig relations[17]. The relative permittivity of the semiconductor is ε_R, the free-space permittivity is ε_o, σ_r and σ_i are the real and imaginary parts, respectively, of the high field conductivity, and ω is the angular frequency of the propagating signal. We should also note that

$$\sigma_R = \frac{Nq^2}{m^*}\left\langle \frac{\tau_m}{1+\omega^2\tau_m^2} \right\rangle \qquad (2.2.2a)$$

and

$$\sigma_i = \frac{Nq^2\omega}{m^*}\left\langle \frac{\tau_m}{1+\omega^2\tau_m^2} \right\rangle \qquad (2.2.2b)$$

where N is the doping level, q is the electronic charge, m^* is the effective mass of the majority carriers, and τ_m is the momentum relaxation time.

For infrared-illuminated GaAs, $\omega^2\tau_m^2 >> 1$ and equations (2.2.2) become

$$\sigma_r = \frac{Nq^2}{m^*\omega^2}\left\langle \frac{1}{\tau_m} \right\rangle \qquad (2.2.3a)$$

and

$$\sigma_i = \frac{Nq^2}{m^* \omega} \quad . \tag{2.2.3b}$$

It is now evident that $\sigma_i >> \sigma_r$, so we neglect the term $\sigma_r^2/\omega^2\varepsilon_o^2$ in (2.2.1). Substituting (2.2.3b), we have

$$n^2 = \varepsilon_R - \frac{Nq^2}{m^* \varepsilon_o \omega^2} \quad . \tag{2.2.4}$$

For two similar semiconducting layers of different doping levels, the square difference in index of refraction can be found as

$$n_1^2 - n_2^2 = (N_2 - N_1)\frac{q^2}{m^* \varepsilon_o \omega^2} \quad . \tag{2.2.5a}$$

In terms of the free-space wavelength, λ_o, (2.2.5a) becomes

$$n_1^2 - n_2^2 = (N_2 - N_1)\frac{q^2 \lambda_o^2}{4\pi^2 \varepsilon_o m^* c^2} \tag{2.2.5b}$$

2.2.2 Mode Selection

To determine which modes will propagate in the etched-channel waveguides, we approximate the structure by a slab waveguide as diagramed in Figure 6. In the experimental structure, n_2 is much greater than n_2' and this limits the mode selection.

The solutions for TE and TM modes in a slab waveguide have been derived by Marcuse[18]. For even TE modes we have the condition,

$$\tan Kd = \gamma/K \quad , \tag{2.2.6a}$$

while for odd TE,

$$\tan Kd = -K/\gamma \quad . \tag{2.2.6b}$$

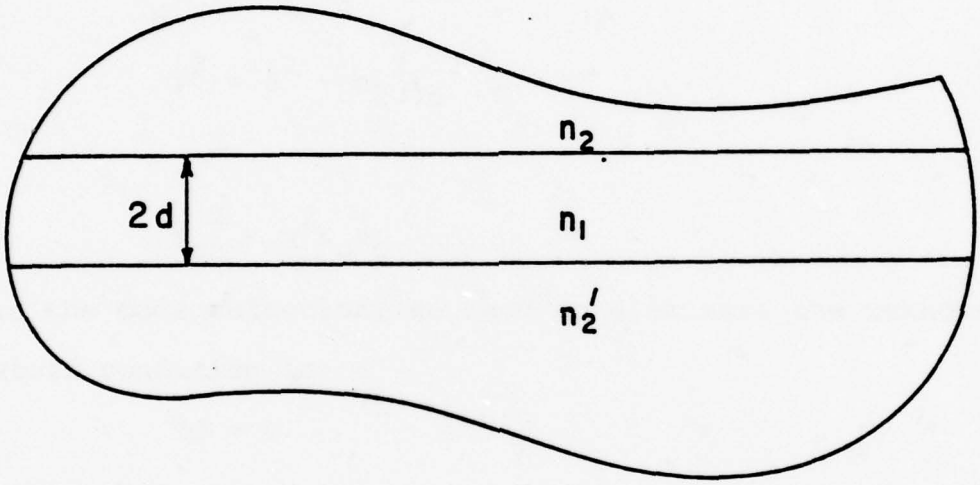

Fig. 6. Structure Used to Derive Mode Selection Rule for the Channel Waveguides.

The condition for even TM modes is,

$$\tan Kd = \frac{n_1^2}{n_2^2} \gamma/k \quad , \tag{2.2.7a}$$

and for odd TM,

$$\tan Kd = -\frac{n_2^2}{n_1^2} K/\gamma \quad . \tag{2.2.7b}$$

Here,

$$K^2 = n_1^2 k_o^2 - \beta^2 \quad , \tag{2.2.8}$$

$$\gamma^2 = \beta^2 - n_2^2 k_o^2 \tag{2.2.9}$$

and

$$k_o^2 = \omega^2 \varepsilon_o \mu_o \quad . \tag{2.2.10}$$

To find the mode selection, we need to eliminate the unknown, β.

The cutoff condition is

$$\gamma d = 0 \tag{2.2.11}$$

at cutoff, then,

$$\beta^2 = n_2^2 k_o^2 \tag{2.2.12}$$

and

$$K = \sqrt{n_1^2 - n_2^2}\, k_o \quad . \tag{2.2.13}$$

Equations (2.2.6) and (2.2.7) are all satisfied by (2.2.11) if

$$Kd = \upsilon\frac{\pi}{2} : \quad \upsilon = 0,1,2,3 \ldots \quad . \tag{2.2.14}$$

Combining (2.2.13) and (2.2.14) gives

$$\upsilon_c = \frac{2}{\pi}\sqrt{n_1^2 - n_2^2}\; k_o d \quad . \tag{2.2.15}$$

Finally, using the results of Section 2.2.1, we find the cutoff eigen value, υ_c ,

$$\upsilon_c \leq \frac{2}{\pi}\sqrt{N_2 - N_1}\; qd\sqrt{\frac{\mu_o}{m^*}} \tag{2.2.16}$$

This result is noteworthy in that υ_c is independent of propagation frequency. It is also evident that the lowest order modes propagate even for evanescent values of $(N_2 - N_1)$.

2.3 Field Effect Transistors

The Schottky-barrier FET structure used in the automatic gain control is shown in Figure 7.

The undepleted channel resistance of this device can be approximated by the bulk resistance of the semiconductor between the source and the drain: that is,

$$R_{CH} = L/aW\sigma_s \quad . \tag{2.3.1}$$

The conductivity of the region, σ_s, is given by

$$\sigma_s \cong qN\mu \quad , \tag{2.3.2}$$

where μ is the mobility of the majority carriers at a doping density N. Therefore, we can express the channel resistance as

$$R_{CH} = L/WaNq\mu \quad . \tag{2.3.3}$$

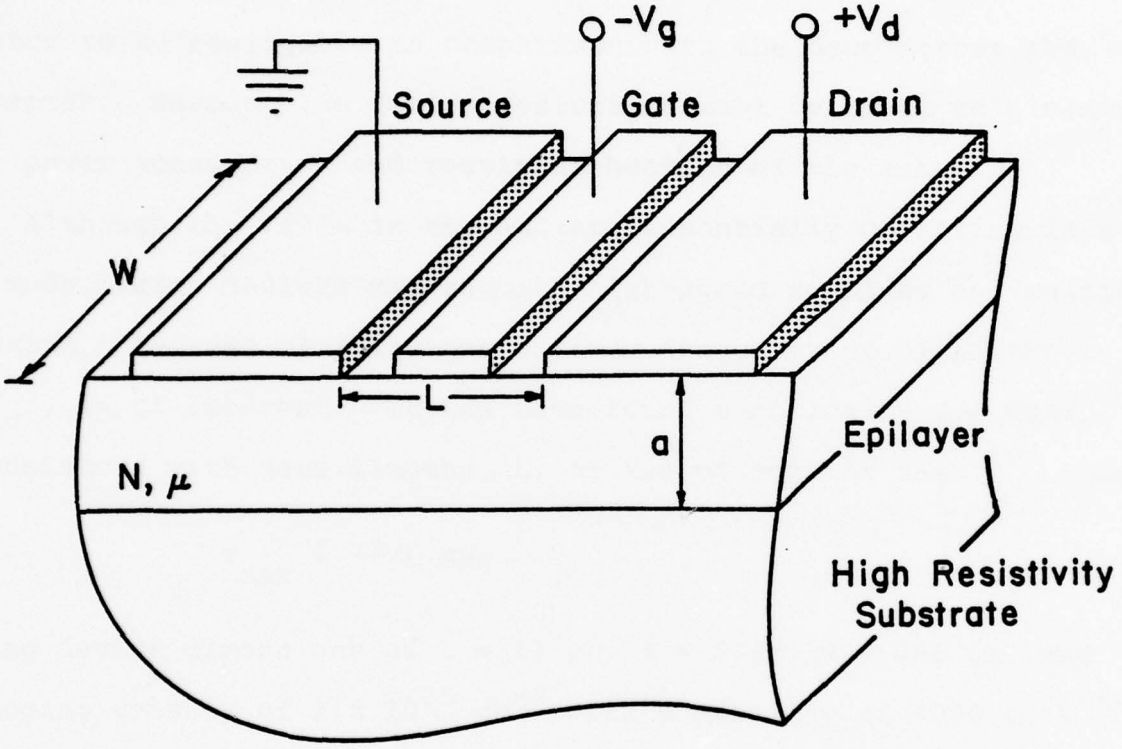

Fig. 7. Schottky Barrier FET Structure.

It is important that this channel resistance be small for two reasons. First, in the AGC operation, the bias across the unilluminated EAP detector must be closely determined to adjust the extent of control. Since the FET is in series with the detector (see Section 2.4), we require the voltage drop across the unbiased transistor to be negligible in comparison with the drop across the detector. Second, the device resistance must be small to minimize the power consumption and resultant heating of the array.

Although the FET's in the AGC are essentially operating in a DC mode, later designs may require high-speed sampling and multiplexing. Because of this, the maximum frequency of oscillation, f_{max}, is of interest. It has been found empirically for GaAs transistors with gate lengths, L, of ten microns or less[19], that

$$f_{max} \cong 33/L \text{ GHz} \quad . \tag{2.3.4}$$

Using device dimensions of L = 10 μm, a = 5 μm, W = 200 μm, and a doping density of 2×10^{15} cm^{-3} with a mobility of 4000 $cm^2V^{-1}s^{-1}$ (see Section 3.1.4), we obtain

$$R_{CH} = 7.8\ \Omega \tag{2.3.5}$$

and

$$f_{max} = 3.3 \text{ GHz} \quad . \tag{2.3.6}$$

These values are well within the requirements of the system.

2.4 Automatic Gain Control

The automatic gain control circuit consists of a feedback loop whereby the gate-to-source voltage of the FET is used as negative feedback to adjust the bias and hence, the responsivity, of an EAP detector. Figure 8 shows the circuit configuration. Coherent illumination of power P through a channel waveguide is incident on an EAP detector biased at voltage V_A. The FET is connected in the common gate configuration. The output of the circuit can be taken as V_A, V_G, or I_L. Resistor R_L is external to the chip, as is the bias supply voltage, V_S.

2.4.1 Operation Below Saturation

In this analysis we use the Shockley model for field effect transistors (20), and neglect the built-in potential of the gate-source junction. The equation for operation below transistor saturation is, then,

$$\frac{I_D}{I_P} = 3\,\frac{V_D}{V_P} - 2\left(\frac{V_D + V_G}{V_P}\right)^{3/2} + 2\left(\frac{V_G}{V_P}\right)^{3/2} . \qquad (2.4.1)$$

Here,

$$I_P = \frac{W_g^{\,2}\mu N_d^{\,2} a^3}{6\varepsilon L} \qquad (2.4.2)$$

and

$$V_P = \frac{qN_d a^2}{2\varepsilon} \qquad (2.4.3)$$

The circuit itself adds the following constraints:

$$I_D = \mathcal{R}P \quad , \qquad (2.4.4)$$

$$V_G = I_D R_L \quad , \qquad (2.4.5)$$

and

$$V_G = \mathcal{R}PR_L \quad . \qquad (2.4.6)$$

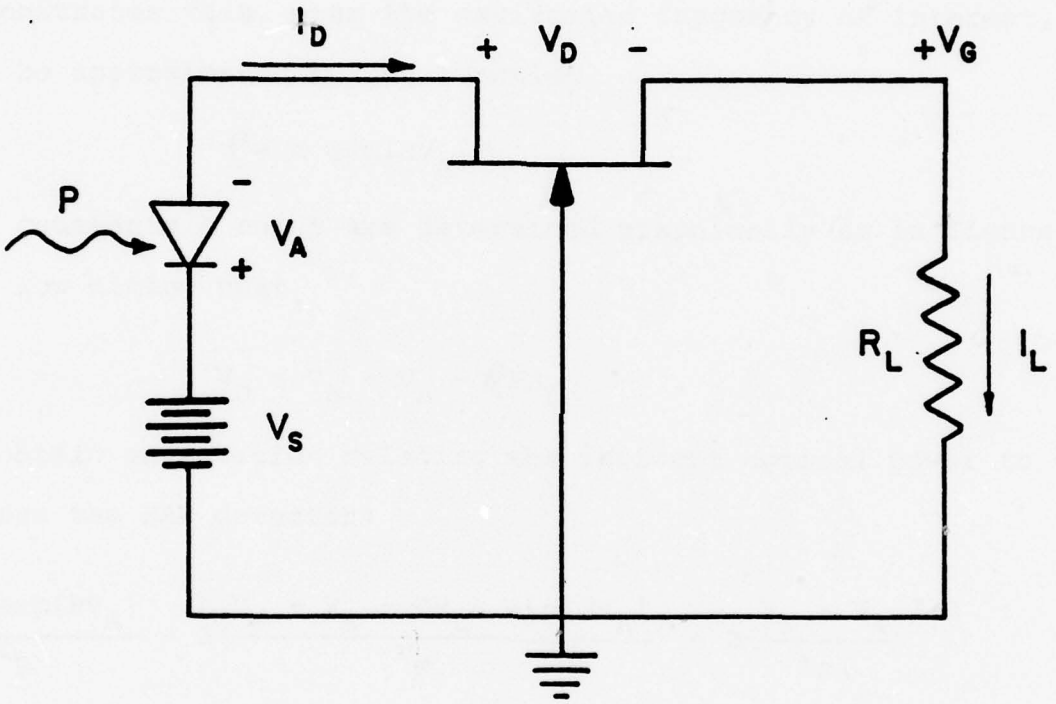

Fig. 8. Automatic Gain Control Circuit.

Substituting these constraints into Equation (2.4.1) gives,

$$\frac{\mathcal{R}P}{I_P} - \frac{3V_D}{V_P} + 2\left(\frac{V_D + \mathcal{R}PR_L}{V_P}\right)^{3/2} - 2\left(\frac{\mathcal{R}PR_L}{V_P}\right)^{3/2} = 0 \quad . \qquad (2.4.7)$$

Equation (2.4.7) is analytically useful only if we can find some closed functional form for $\mathcal{R}$. The responsivity data of Sun et al.[2] demonstrates that, near the excitation frequency of interest, $\mathcal{R}$ can be approximated by the function

$$\mathcal{R} = A \exp[BV_A] \quad . \qquad (2.4.8)$$

The constants A and B are determined graphically as in Figure 9.

Now noting that

$$V_D = V_S - V_A - \mathcal{R}PR_L \quad , \qquad (2.4.9)$$

we obtain an equation relating the incident optical power to the bias across the EAP detector:

$$\frac{PA \exp[BV_A]}{I_P} - 3\left(\frac{V_S - V_A - PR_LA \exp[BV_A]}{V_P}\right) + 2\left(\frac{V_S - V_A}{V_P}\right)^{3/2}$$

$$-2\left(\frac{PR_LA \exp[BV_A]}{V_P}\right)^{3/2} = 0 \qquad (2.4.10)$$

Some solutions of this equation for various values of V_S and R_L are plotted in Figure 10. Values of 6 milliamps and 1.2 volts were used for I_P and V_P, respectively.

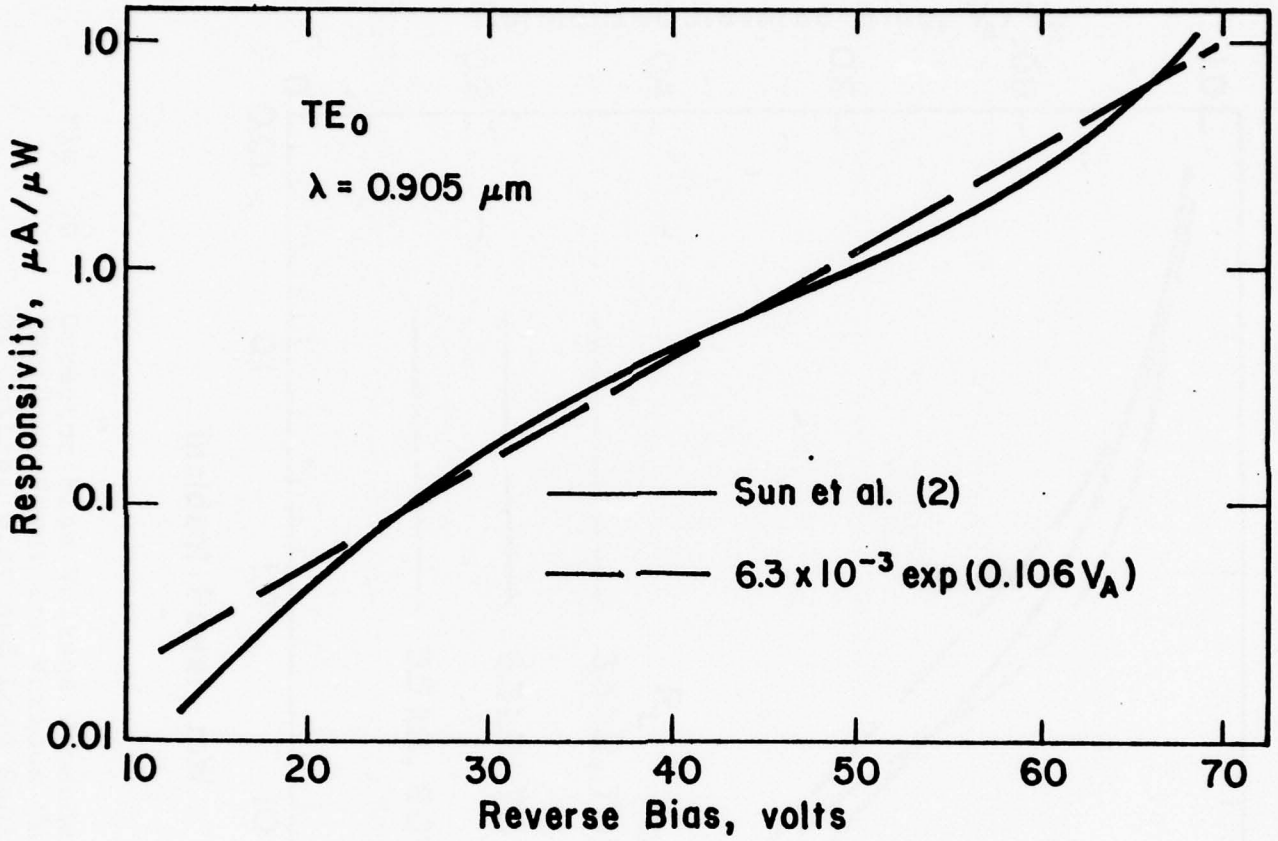

Fig. 9. Functional Approximation to Responsivity Data of Sun et al.[2] at 0.905 μm Illumination.

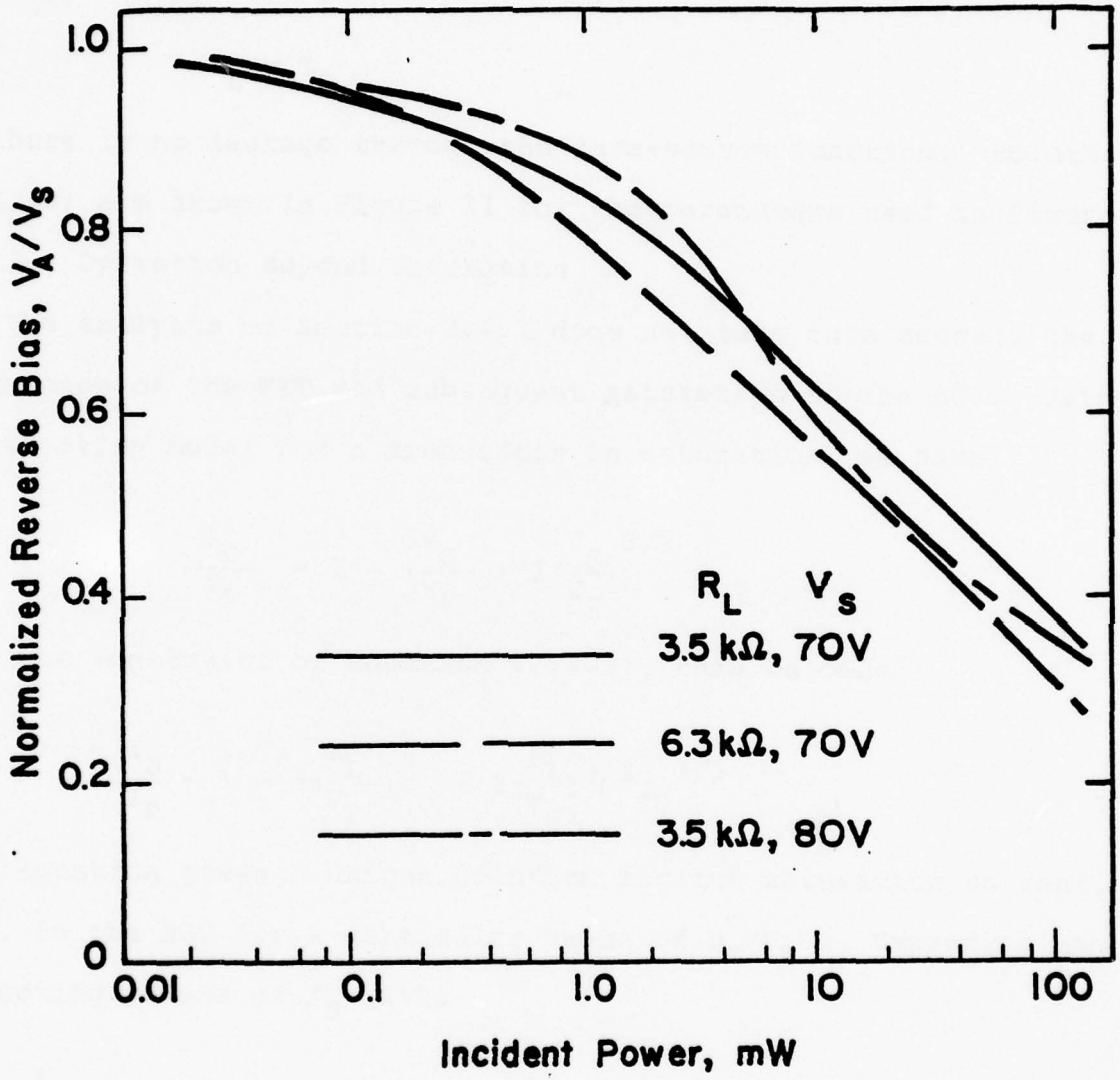

Fig. 10. Detector Bias Voltage Dependence on Incident Power for Various Values of Initial Bias and Load Resistor.

Equation (2.4.10) can also be used to find I_L as a function of the input power. Once V_A is found for a value of P , Equations (2.4.4) and (2.4.8) determine the load current since

$$I_L = I_D \tag{2.4.11}$$

if there is no leakage through the gate-source junction. Solutions of $I_L(P)$ are shown in Figure 11 for the parameters used in Figure 9.

2.4.2 Operation Beyond Saturation

The analysis of Section 2.4.1 does not take into account the saturation of the FET and subsequent saturation of the AGC. Using the Shockley model for a transistor in saturation, we have

$$\frac{I_D}{I_P} = 1 - \frac{3V_G}{V_P} + 2\left(\frac{V_G}{V_P}\right)^{3/2} . \tag{2.4.12}$$

With the constraint of Equation (2.4.5), this becomes

$$\frac{I_D}{I_P} = 1 - 3\left(\frac{R_L}{V_P}\right) I_D + 2\left(\frac{R_L}{V_P}\right)^{3/2} I_D^{3/2} . \tag{2.4.13}$$

This equation gives a unique solution for the saturation current, I_{DS} , in the AGC for a particular value of R_I/V_P . Expanding and collecting powers of I_D gives

$$4\left(\frac{R_L}{V_P}\right)^3 I_{DS}^3 - \left[\frac{1}{I_P^2} + \frac{6}{I_P}\left(\frac{R_L}{V_P}\right) + 9\left(\frac{R_L}{V_P}\right)^2\right] I_{DS}^2 + \left[\frac{2}{I_P} + 6\left(\frac{R_L}{V_P}\right)\right] I_{DS} = 1 \tag{2.4.14}$$

If R_L is on the order of kilohms, V_P is a few volts, and I_P is a few milliamps, then the higher order terms in R_I/V_P will dominate and a simple cubic equation is left:

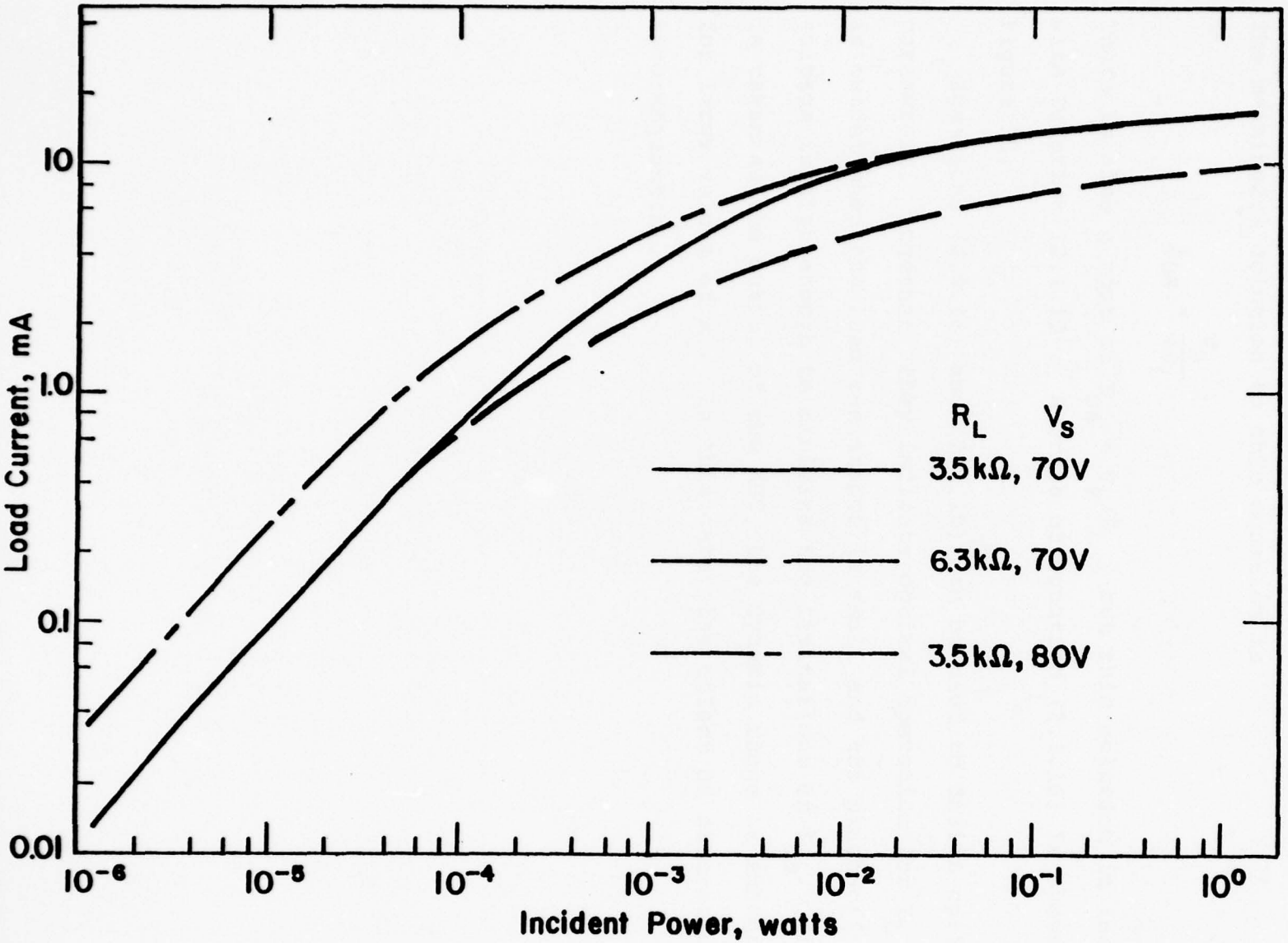

Fig. 11. Load Current Dependence on Incident Power for Various Values of Initial Bias and Load Resistor.

$$4\left(\frac{R_L I_{DS}}{V_P}\right)^3 - 9\left(\frac{R_L I_{DS}}{V_P}\right)^2 + 6\left(\frac{R_L I_{DS}}{V_P}\right) - 1 = 0 \quad . \tag{2.4.15}$$

The meaningful solution to this equation is

$$I_{DS} = \frac{V_P}{4R_L} \quad . \tag{2.4.16}$$

There is also a root at $I_{DS} = V_P/R_L$, but this solution is inconsistent with Equation (2.4.13). A graph of equation (2.4.16) is shown in Figure 12.

Equations (2.4.16) and (2.4.10) can be used to design optimum AGC parameters. Together, they indicate optimal operation for I_L taken as output when the load resistance is small and the pinch-off voltage is high enough to minimize the limitations of I_{DS}. If V_A is taken as the output of the AGC, the dynamic range is enhanced for large values of R_L. In this case, the effect of saturation is inconsequential.

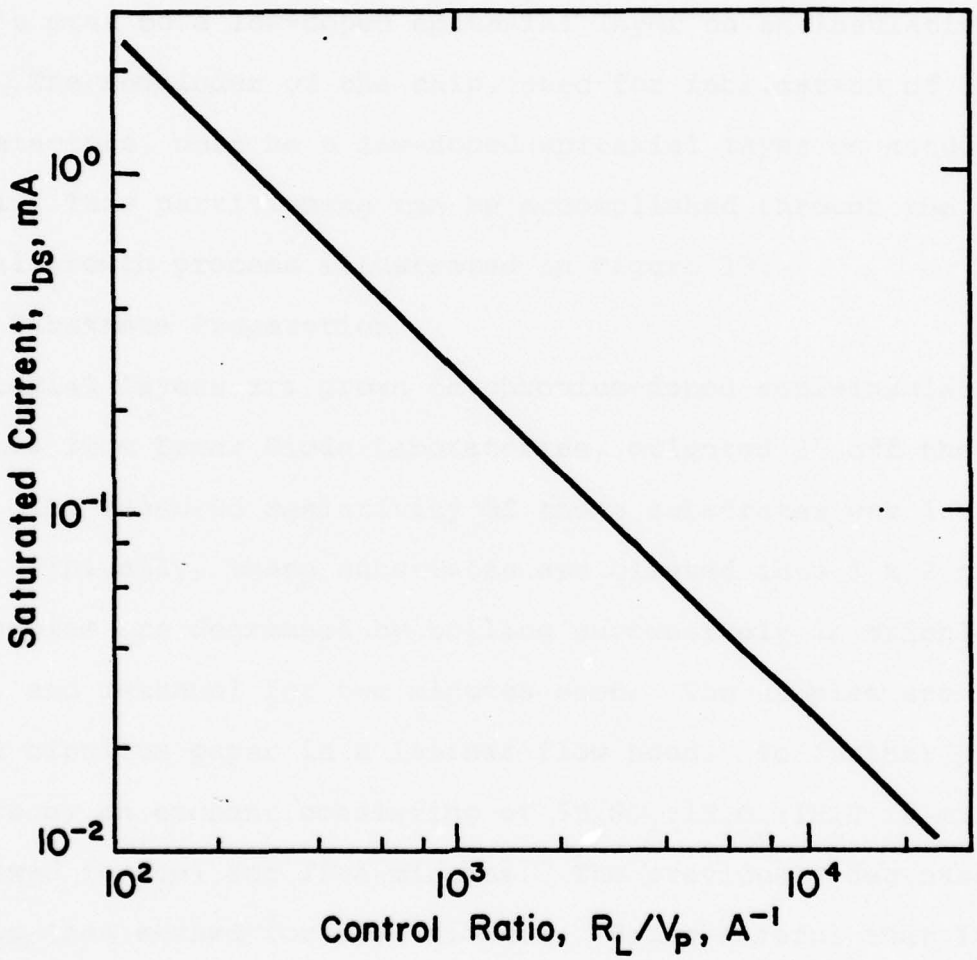

Fig. 12. Maximum AGC Current with the FET Driven into Saturation.

3. FABRICATION

3.1 Epitaxy

Monolithic integration of FET's and detectors requires a chip with two epitaxial regions. The portion of the chip intended for the FET's must be a low-doped epitaxial layer on an insulating substrate. The remainder of the chip, used for fabrication of the waveguide detectors, must be a low-doped epitaxial layer on conducting material. This partitioning can be accomplished through the double epitaxial growth process illustrated in Figure 13.

3.1.1 Substrate Preparation

Epitaxial layers are grown on chromium-doped semi-insulating substrates from Laser Diode Laboratories, oriented 2° off the {100} planes. The measured resistivity of these substrates was 1×10^{7} ohm-cm. Typically, these substrates are cleaved into 1 x 2 cm pieces. These samples are degreased by boiling successively in trichloroethylene, acetone, and methanol for two minutes each. The samples are then dried in bibulous paper in a laminar flow hood. To further prepare the surface, an etchant consisting of $5H_2SO_4:1H_2O_2:1H_2O$ is mixed and allowed to cool for five minutes. The previously degreased sample is then etched for five minutes. Being careful that it is not exposed to air to prevent oxidation of the surface, the sample is rinsed in water deionized to a resistivity of at least 14 megohm-cm. Drying is done with bibulous paper in a laminar flow hood.

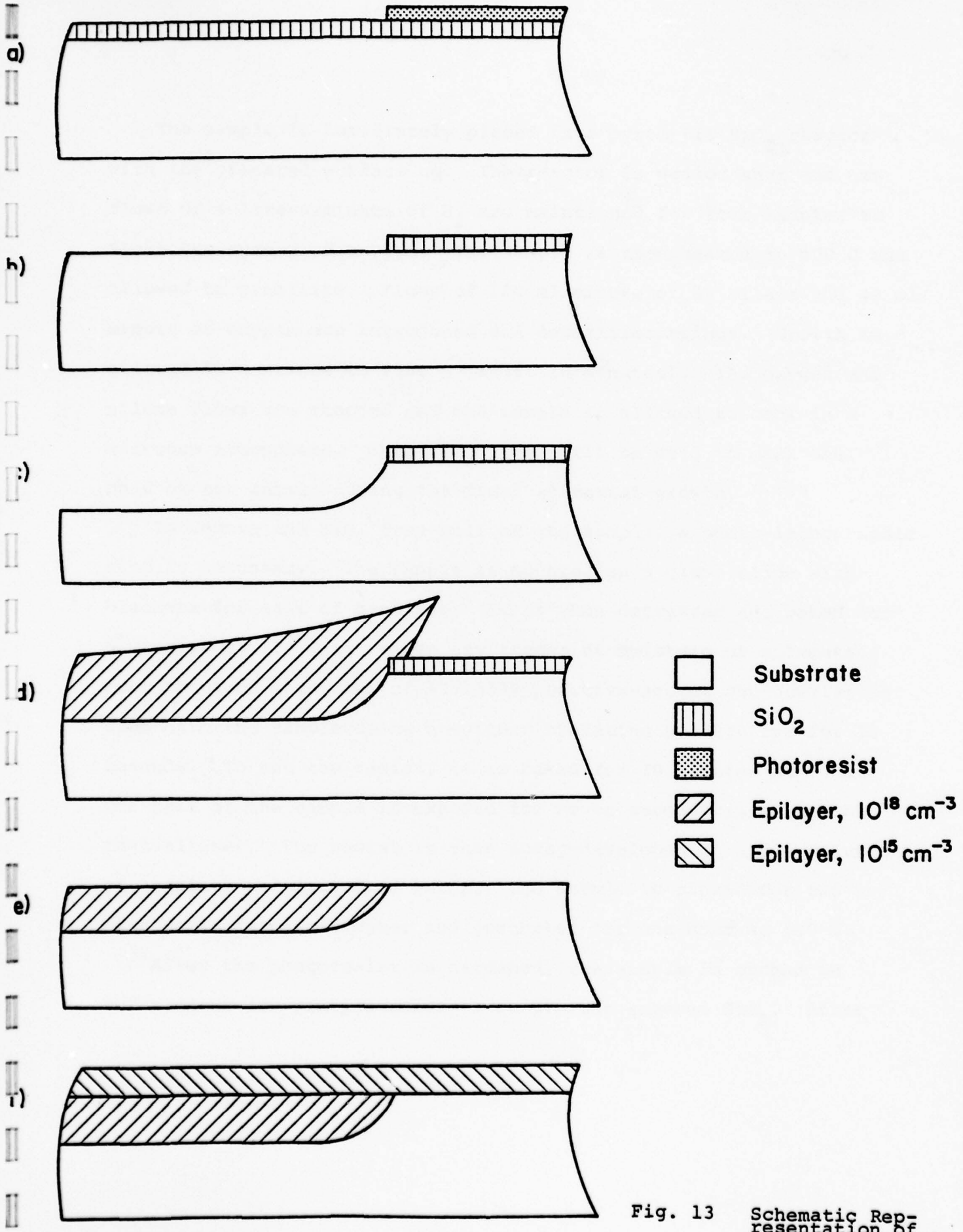

Fig. 13 Schematic Representation of double Epitaxial Growth.

The sample is immediately placed in a pyrolytic SiO_2 reactor with the prepared surface up. The reactor is sealed shut and two flows of 4 liters/minute of N_2 are maintained for four minutes to flush the system of oxygen. The sample is then heated to 400 C and allowed to stabliize. Flows of 100 ml/minute of 5% silane and 40 ml/minute of oxygen are introduced and deposition beings. Growth is allowed to continue to 2500 $\mathring{A}$ (about 10 minutes). The oxygen and silane flows are stopped and the sample is allowed to cool in a nitrogen atmosphere. This SiO_2 layer will be used to mask one half of the sample during the first epitaxial growth.

To remove the SiO_2 from half of the sample, a photo-lithographic step is necessary. The sample is mounted on a glass slide with blackwax for ease of handling. It is then degreased and baked for 5 minutes at 130 G to remove any traces of moisture or solvents. Four thousand Angstroms of AZ 1350B positive-acting photoresist is spun onto the sample using a spinner operating at 3000 rpm for 30 seconds. To set the resist, it is baked for 20 minutes at 70 C. One half of the sample is exposed for seven seconds in an optical mask aligner. The resist is then spray-developed in a 50% solution of Azoplate and deionized water. The sample is rinsed for two minutes in deionized water and postbaked for one hour at 100 C.

After the photoresist is hardened, the sample is etched in buffered-HF for sixty seconds to remove the exposed SiO_2. After

being rinsed in deionized water, the sample is gently heated to remove it from the glass slide. The photoresist and blackwax are removed simultaneously by sequential boiling in trichloroethylene, acetone, and methanol. The $5H_2SO_4:1H_2O_2:1H_2O$ etch is prepared and cooled for four minutes. The sample is etched for six minutes, rinsed in deionized water, and dried in bibulous paper.

This procedure produces a 30 μm valley over half the sample and leaves SiO_2 covering the other half. This SiO_2 layer will prevent growth so that only the valley half of the sample will nucleate the first epitaxial layer. A schematic of the process is shown in Figures 13 a-c.

3.1.2 First Epitaxial Growth

The epitaxial reactor used to grow the layers is a vapour-phase $AsCl_3:Ga:H_2$ system as indicated in the diagram of Figure 14. The furnace is a single winding which is connected to provide two independent zones. Each zone is controlled by its own solid state temperature controller. The furnace tube, boat, $AsCl_3$ bubbler and seedholder are all fashioned of Spectrosil and fused quartz to insure low contamination. The system is airtight with access through a taper joint in which the seedholder is mounted. The $AsCl_3$ bubbler is surrounded by a constant temperature bath controlled by a refrigerated circulator.

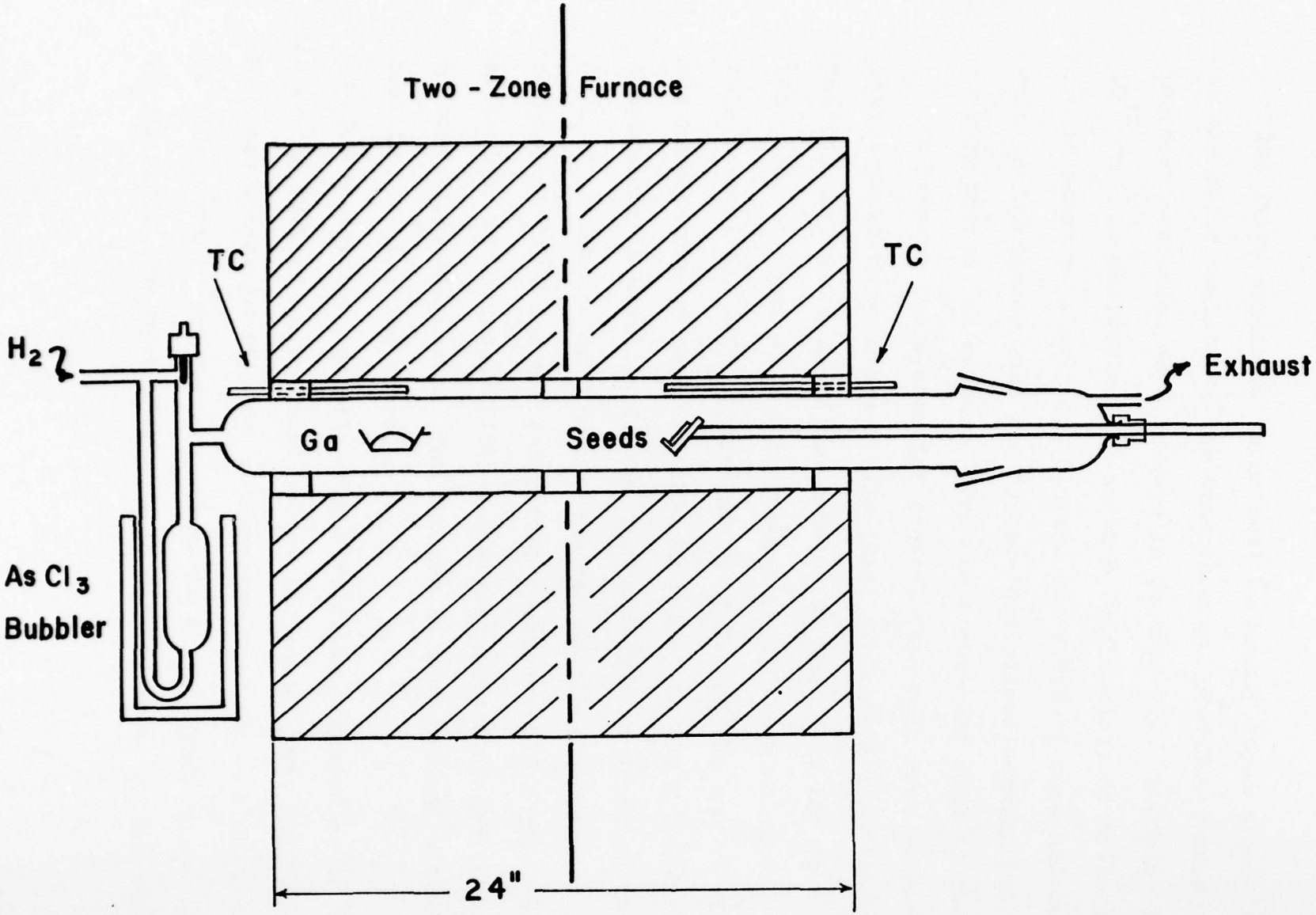

Fig. 14. The Epitaxial Reactor Used to Grow GaAs Layers.

The first epitaxial layer must be highly doped since it serves as the ohmic contact to the detectors and provides guiding of the incident radiation as discussed in Section 2.2. A doping level of 10^{18} cm^{-3} is desirable. To achieve this doping, 82 milligrams of tin is added to a melt of 10 grams of 99.9999+% pure gallium. This melt is introduced into the furnace and placed between the 16 and 19 inch points, as measured from the right-hand edge of the furnace.

To prepare the system for growth, this melt must be saturated with arsenic to generate a GaAs skin. This is accomplished by pre-heating the melt side of the furnace to 840 C and the seed side to 700 C for $3\frac{1}{2}$ hours with a hydrogen flow of 150 ml/minute. During this warmup, the $AsCl_3$ is cooled to 12 C. At the end of $3\frac{1}{2}$ hours, the temperature on the seed side is raised to 800 C. When the temperature is stabilized, the hydrogen flow is diverted through the $AsCl_3$. At the end of 3 hours, the temperature on the seed side is reduced to 735 C and the saturation continues for 3 more hours. At that time, the hydrogen flow is diverted away from the $AsCl_3$ and reduced to 30 ml/minute. The furnace is shut off and allowed to cool for at least 10 hours.

Growth may now proceed. The substrate, prepared as in Section 3.1.1 is mounted on the seed holder and sealed into the furnace. The seed holder is adjusted so that the seed sits at the 5 inch point. At this point in the furnace, there is a 15 C gradient on each side of the seed. The system is flushed with hydrogen at the rate of

250 ml/minute for 15 minutes. The hydrogen flow is then reduced to 150 ml/minute and the furnace is preheated as for saturation. The $AsCl_3$ is cooled to 6 C to prevent formation of hillocks. After $3\frac{1}{2}$ hours, the temperature on the seed side is raised to 800 C and allowed to stabilize for 15 minutes. The hydrogen is diverted through the $AsCl_3$ and an etch cycle begins. After 15 minutes, approximately 5 μm of the substrate surface has been removed, and the seed temperature is reduced to 740 C. After 20 minutes, growth begins and continues for six hours. The hydrogen flow is then diverted from the $AsCl_3$ and reduced to a flow rate of 30 ml/minute. The furnace is allowed to cool and the seed is removed. This growth procedure results in a 35-40 μm layer being grown on the unmasked portion of the seed crystal. As shown in Figures 13 and 15, considerable overgrowth occurs at the interface between the masked and unmasked regions of the crystal.

3.1.3 Preparation for Second Epitaxial Growth

The overgrowth described in the previous section must be removed before the second epitaxial layer can be grown. A specially designed jig, shown in Figure 16, is used as a sample mount. Float plate glass, 6" x 6" x $\frac{1}{4}$", is used as a polishing block.

To prepare the plate glass for polishing, at least four pieces are required. Each pair is polished optically flat by grinding them

Fig. 15. Overgrowth at Interface Between Masked and Unmasked Regions.

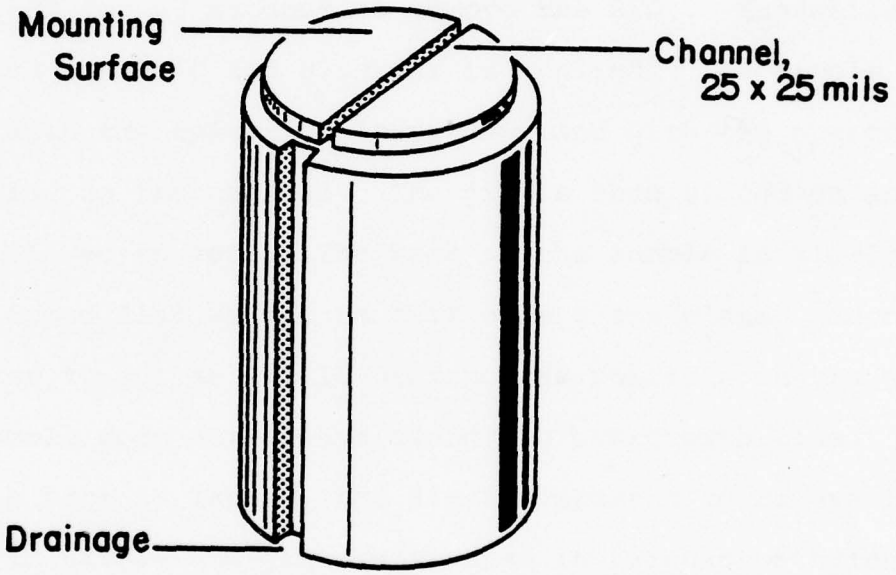

Fig. 16. Jig Used for Mounting Sample During Removal of Overgrowth.

together, successively, with 25, 5, and 2 μm grits. The surface of the jig is then polished against one pair of these plates with 25 and 5 μm grits. The flatness of the jig is determined by comparison with a standard knife edge. Using this method, the jig can be made flat to within a few micrometers.

The overgrowth can now be removed. Any GaAs nucleation on the SiO_2 side of the sample is first removed. The sample is then etched in buffered-HF for 60 seconds to remove the SiO_2. Meanwhile, the jig is heated to 100 C and blackwax is applied. The sample is mounted on the jig with the epitaxial layer down and with the overgrowth region resting in the channel. The jig is then placed on an aluminum plate and allowed to cool. The back of the sample is slowly and carefully lapped flat with 2 μm grit on a glass plate. Much care must be taken to put as little pressure as possible on the jig so that the sample does not cleave along the overgrowth line.

When the back is lapped, the jig is reheated to remove the sample. Both sample and jig are cleaned in trichloroethylene, acetone, and methanol to remove all traces of blackwax. The sample is remounted with the lapped face against the jig. A very thin slurry of 2 μm grit is spread over the last glass plate. The sample is pushed through this slurry once or twice and then examined under the microscope. If only the overgrowth is lapped, then the sample is mounted correctly and the next step may begin. If, however, the

overgrowth and one edge of the sample are lapped, then the sample is incorrectly mounted and appropriate adjustments must be made.

The next step is to take the correctly mounted sample and to polish it chemically-mechanically in a 1% solution of bromine in methanol. The solution is sprayed on a napless nylon mat mounted on a rotating polishing wheel. Very little pressure is applied as the sample is held against this mat. The sample is periodically checked under low magnification to see when the overgrowth has been removed. The total polishing time is about one-half hour.

The sample is demounted and degreased. The $5H_2SO_4:1H_2O_2:1H_2O$ etch is prepared and allowed to cool for ten minutes. The sample is etched for 15 seconds, rinsed in deionized water and dried in bibulous paper. It is now ready for the growth of the second epitaxial layer. The process is diagramed in Figures 13 d and e.

3.1.4 Second Epitaxial Growth

The second epitaxial layer is low-doped to accommodate both the FET's and waveguide detectors. The desired doping level is 1×10^{15} cm^{-3}.

A melt to produce this doping level is prepared by placing three 10 mil tin spheres in a 10 gram ingot of gallium and saturating as in Section 3.1.2. The seed prepared in the previous section is mounted on the seed holder, which is adjusted to rest at the 5 inch point. Times and temperatures are the same as for the first epitaxial growth,

except that growth is allowed to proceed for only 70 minutes before the reactor is shut down. This growth time produces a layer 5 μm thick. The resulting structure is shown in Figure 13 f.

3.2 Waveguide Detectors

The waveguide detector structure to be fabricated is illustrated in Figure 17. The aluminum Schottky barrier EAP detectors are 100 μm x 20 μm. The channel waveguides are 20 μm wide and 5 μm high on 40 μm centers. They are cleaved on a {110} plane to a length of 1 mm. The waveguide epitaxial layer is nominally doped at 1×10^{15} cm^{-3} with the contact layer at 1×10^{18} cm^{-3}. With these design parameters, we expect (see Section 2) a breakdown voltage of about 100 volts. The difference in squared indices of refraction of the two layers at an illumination wavelength of 0.905 μm is 0.0109. Consequently, the cutoff eigen value, v_c, is unity, and we expect only TE_o, TM_o, TE_1, and TM_1 modes to propagate in the waveguides.

To begin fabrication of this structure, the double epitaxial sample is coated with 2500 Å of SiO_2 as described in Section 3.1.1. Photoresist AZ 1350B is deposited as in that section, and the waveguide portion of the crystal is exposed, developed and rinsed. The SiO_2 is etched in buffered-HF for 60 seconds, and the photoresist is removed in acetone. This leaves a thick protective layer of SiO_2 over the half of the sample that will be processed for FET's. The sample is then mounted on a glass slide and degreased. To prepare

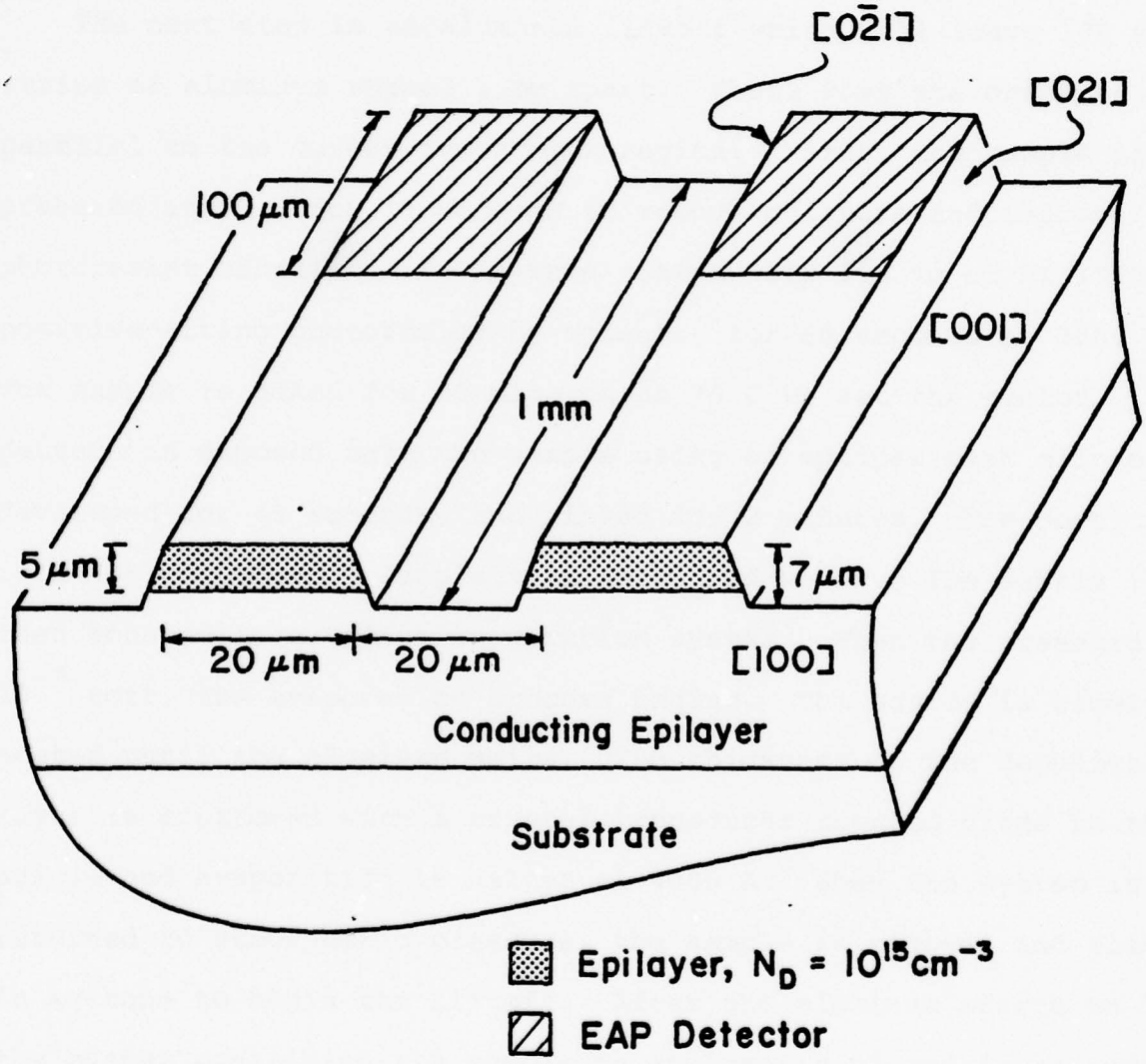

Fig. 17. The Channel Waveguide Structure with EAP Detectors.

the surface for processing, the $5H_2SO_4:1H_2O_2:1H_2O$ etch is prepared and cooled for 10 minutes. The sample is etched for 5 seconds and rinsed. It is then dipped for 15 seconds in HCℓ and rinsed. This step removes the effects of any accidental oxide formation.

The next step is an aluminum liftoff which will leave 100 μm strips of aluminum spaced 1 mm apart. These rows are oriented parallel to the former overgrowth region. First, the sample is prebaked at 85 C for 15 minutes to remove moisture and improve photoresist adhesion. It is then coated with 1.4 μm of AZ 1350J positive-acting photoresist by spinning for 60 seconds at 3000 rpm. The sample is baked for 20 minutes at 70 C to set the resist. The pattern is exposed onto the sample using an optical mask aligner, developed for 45 seconds, and rinsed for 2 minutes. The developer is a 50% solution of Azoplate in deionized water. The sample is then mounted in a vacuum evaporation system. When the pressure is 10^{-7} torr, the evaporation process begins. The source is slowly heated until the aluminum melts. The thickness of the deposited layer is monitored with a crystal transducer mounted close to the sample and evaporation is halted at 4000 Å. When the system is returned to atmospheric pressure, the sample is removed and soaked in acetone to begin the liftoff. After the aluminum starts to lift, the beaker containing the sample in acetone is placed in an ultrasonic bath to complete the process.

The waveguide structures can now be delineated. The sample is removed from the glass slide and degreased. It is then covered with 1100 Å of pyrolytic SiO_2 using the procedure indicated in Section 3.1.1. When the sample is removed from the reactor, it is remounted and baked for 5 minutes at 105 C. A layer of AZ 1350J is spun on at 3000 rpm for 30 seconds. After the bake to set, the resist is exposed for 6 seconds, developed for 45 seconds, rinsed for 2 minutes, and baked for 1 hour at 105 C. The SiO_2 must now be etched to reproduce the pattern. Three beakers are used for this procedure: two contain deionized water and one contains buffered-HF. The crystal is dipped in one beaker of water, etched for 5 seconds in the buffered-HF, then dipped in the second beaker of water. This is repeated, then repeated again for 4 seconds of etch. Next, the aluminum is removed between the waveguides to delineate the EAP detectors. The aluminum etch is a 1:12 dilution of Aurostrip in deionized water. The etch is heated to 38 C and allowed to stabilize. Nitrogen is bubbled through the solution by way of a ceramic disk bubbler to create a foam. The sample is held in this foam to etch for 5 minutes. It is then rinsed thoroughly in deionized water and the photoresist is removed in acetone. The channels themselves are etched by preparing a $5H_2SO_4:1H_2O_2:1H_2O$ etch and cooling it for 9 minutes. The sample is etched for one minute. A rinse in deionized water completes the process, which is diagramed in Figure 18.

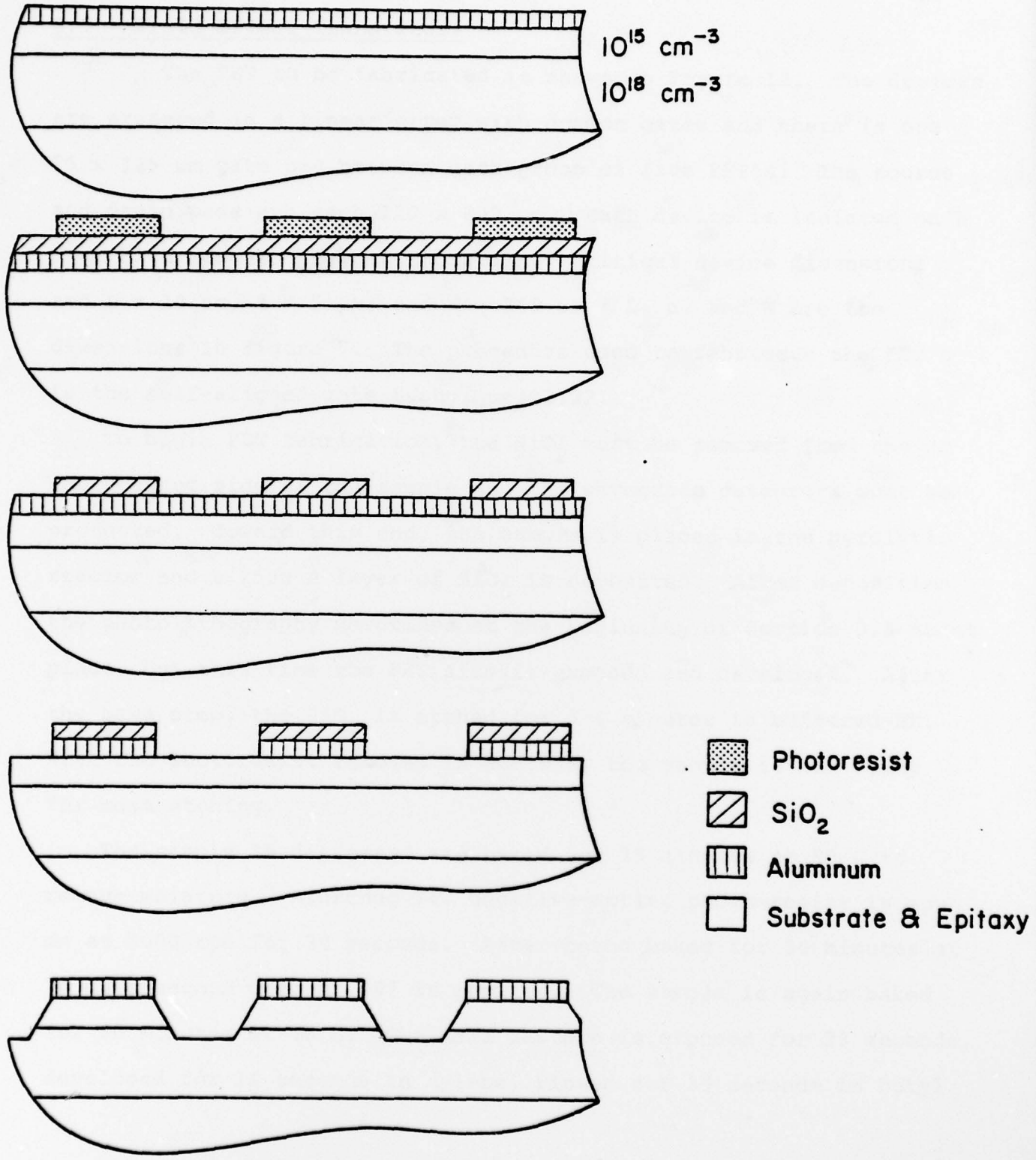

Fig. 18. Fabrication of Waveguide Detectors

3.3 Field Effect Transistors

The FET to be fabricated is shown in Figure 19. The devices are arranged in a linear array with common gates and there is one 75 x 125 μm gate pad between each group of five FET's. The source and drain pads are each 120 x 200 μm. Each device is isolated on a 7 μm high mesa to prevent crosstalk. Critical device dimensions are L = 10 μm, a = 5 μm, and W = 200 μm. L, a, and W are the dimensions in Figure 7. The procedure used to fabricate the FET's is the self-aligned gate technique(21,22).

To begin FET fabrication, the SiO_2 must be removed from the unprocessed side of the sample and the waveguide detectors must be protected. Toward this end, the sample is placed in the pyrolytic reactor and a 2500 Å layer of SiO_2 is deposited. After deposition the photolithography described at the beginning of Section 3.2 takes place, but this time the FET side is exposed and developed. After the bake step, the SiO_2 is etched for 3-4 minutes in buffered-HF. With the photoresist removed in acetone, the sample is now ready for mesa etching.

The sample is degreased and baked for 15 minutes at 85 C to remove moisture. Microneg 747 negative-acting photo-resist is spun on at 5000 rpm for 30 seconds. After being baked for 30 minutes at 70 C, a second coat of 747 is applied. The sample is again baked for 30 minutes at 70 C. The mesa pattern is exposed for 23 seconds, developed for 15 seconds in xylene, rinsed for 30 seconds in butyl

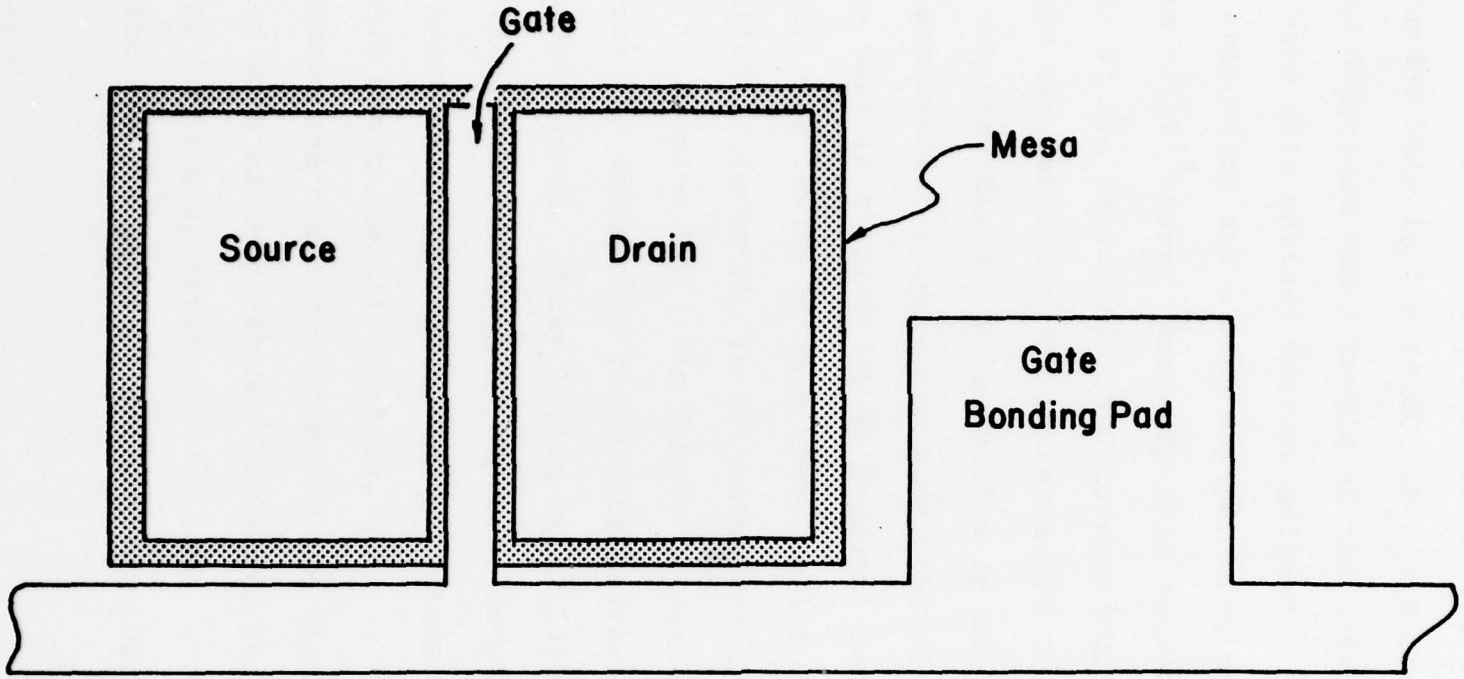

Fig. 19. Top View of FET Showing Position of the Gate Bonding Pad.

acetate and postbaked for 30 minutes at 130 C. The pattern is then etched for 1 minute in the $5H_2SO_4:1H_2O_2:1H_2O$ etch cooled for 9 minutes. A rinse in deionized water completes the mesa fabrication.

Next, the gate pattern must be defined. The sample is loaded into the evaporator and a 5000 Å layer of aluminum is deposited at a pressure of 10^{-7} torr. The sample is removed and baked for 15 minutes at 85 C. Resist AZ 1350J is spun onto the sample for 60 seconds at 6600 rpm and baked for 30 minutes at 70 C. The spin and bake is repeated two more times. This results in the very thick (~3 μm) layer of photoresist required to cover the edge of the mesa. The rough gate mask is exposed for 45 seconds, developed for 60 seconds and rinsed. The sample is then baked at 110 C for 90 minutes. A 1:12 dilution of Aurostrip in deionized water is heated to 36 C and foamed as in Section 3.2. The sample is placed in the foam for 10-20 minutes to define the rough gate pattern. The final gate step can now be performed. Three layers of AZ 1350J are deposited as before. The final gate mask is exposed, developed, rinsed, and baked. The 1:12 Aurostrip etch is prepared as before and the pattern is etched 15-20 minutes until complete.

The source and drain contacts are the final additions. They are applied with an evaporation, lift-off, and alloy. A 1500 Å layer of Au-Ge is evaporated at 10^{-7} torr. This layer is then covered with a 400 Å layer of evaporated nickel. The second

evaporation is necessary to retain the Au-Ge eutectic during the contact alloy. The lift-off is begun by soaking the sample in acetone and then momentarily placing it in the ultrasonic bath to remove the metallization. The sample is then degreased. Finally, the contacts are alloyed at 450 C for 20 seconds in a H_2 atmosphere. This completes the FET fabrication process, which is diagramed in Figure 20.

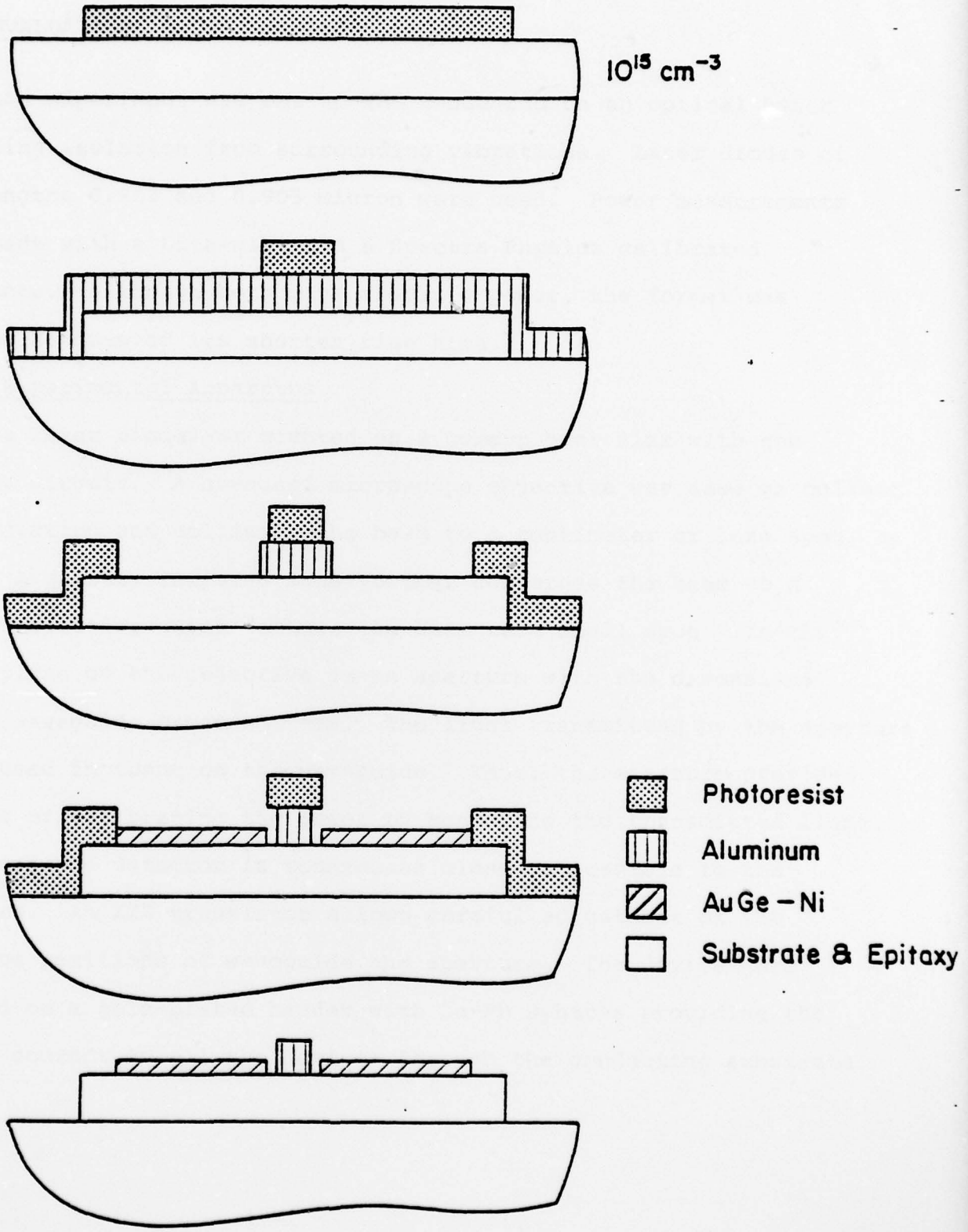

Fig. 20. Fabrication of the FET's by the Self-aligned Gate Technique.

4. EVALUATION

This experiment was set up and conducted on an optical bench providing isolation from surrounding vibrations. Laser diodes of wavelengths 0.904 and 0.905 micron were used. Power measurements were made with a Lite-mike and a Spectra Physics calibrated detectors. Although both gave absolute power, the former was favored because of its shorter rise time.

4.1 Experimental Apparatus

The laser diode was mounted on a common heat sink with the driving circuit. A standard microscope objective was used to collect the radiation and collimate the beam to a centimeter or less spot size. A quartz, infrared lens further converges the beam to a second objective which focuses the beam to a small spot. In the focal plane of the objective is an aperture with the dimensions of the waveguide cross-section. The light transmitted by the aperture is assumed incident on the waveguide. Thus, the aperture provides a means of calibrating the power by measuring the transmitted light. The waveguide detector is mounted as close as possible to the aperture. An XYZ translator allows careful adjustment of the relative positions of waveguide and aperture. The devices are mounted on a gold-plated header with Sn-Pb spheres providing the common contact to all the devices through the conducting substrate.

Two tungsten whisker probes are located on independent positioners above the devices where their position can be observed with a stereo microscope. Initially, the detector is placed in series with a voltage source and a 50 ohm resistor. The voltage across the resistor is monitored on a scope as a measure of the device current. For the AGC circuit, the 50 ohm resistor is replaced with a GaAs FET and load resistor, R_1.

4.2 Experimental Procedure

The laser was set up with the associated optics and its output was optimized with the power meter. The 0.905 micron lasers operated at a pulse repetition frequency (PRF) of 100 Hz and a pulse width of 700 nsec. Operation was essentially LED, giving only a few milliwatts output. After passing through the aperture, the power was reduced to 78 microwatts. The power was measured for various laser currents and a calibration curve plotted. At this time, a sample was placed in the moveable stage and an optimum device chosen. The stage was then aligned with the beam for maximum device response. The laser current was varied and the resulting response measured. Responsivity was calculated after accounting for the reflection loss at the waveguide face and the absorption in the waveguide. This was repeated at other bias voltages and compared. At maximum laser power, the bias voltage was varied and the resulting photoresponse recorded.

4.3 Difficulties Encounterd

Initially only two 0.905 micron lasers were available for the evaluation of the detector array with AGC. Although the power output was only a few milliwatts, these were used to measure photo-response versus laser power. Problems soon arose when the laser power was decreased as detection of the current became marginal. The oscilloscope in use was limited to 5 mv/cm which for a 50 ohm load requires 100 μamps. The limiting power then was about one-half μwatt, giving a power range of 23 dB. Attempts were made to extend the range downward with pulse amplifiers and increases in the 50 ohm load. The use of amplifiers required calibration and matching to the 50 ohm load. Under these conditions, noise in the circuit was of the same order as the signal. This noise was also apparent when the load resistor was increased in size. Detector response time also suffered greatly due to the increased circuit resistance. Noise was found to originate in the laser driving circuit and attempts to shield it did not help.

Apparently the laser diodes had degraded from use at too large a duty cycle. Two 0.904 micron lasers were then obtained and operated below the maximum ratings so as to prolong life. Without the aperture these diodes produced close to one watt of power. With the aperture, transmitted light was barely detectable. By changing from the LED to the lasing mode, focusing was not adequate for

transmission. Different schemes were tried to correct and improve the transmission, but with little success. It is possible that the extreme convergence required for a small beam waist causes the beam to diverge before entering the lite-mike. This would make the aperature useless for calibrating the incident power. When the laser was focused directly on the waveguide, a large response was observed in excess of one ma. Obviously, the power was there, but was difficult to calibrate for absolute measurements. This problem must be solved to achieve the required 50 dB range of power and complete the evaluation.

4.4 Results

The difficulties mentioned above limited the measurements to a 23 dB range of incident power. Responsivity was calculated from the response data by accounting for the reflection loss at the waveguide face and absorption along its length. That is,

$$P_a = P_i(1 - R)\exp(-\alpha \ell)$$

where

P_a = power at detector,

P_i = total power incident,

α = absorption coefficient,

ℓ = length along waveguide, and

the responsivity is

$$R = \frac{I_p}{P_a} \text{ in amps/watt.}$$

In this manner responsivities as high as 600 amps/watt were obtained at optimum reverse bias voltage. The crosstalk between channels was limited by the measurement difficulties discussed above.

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